MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2015/2016

DCS5158 – COMPUTER ARCHITECTURE

(DIT Students Only)

3 JUNE 2016
9.00 AM to 12.00 PM
(3 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of 7 pages with 2 sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer ALL the questions in this section and shade your answers on the OMR sheet provided.*

1. Which of the following are the main functions performed by a computer?
   I. Data processing
   II. Data storage
   III. Data movement
   IV. Control

   A. I and II
   B. I, II and II
   C. I, III and IV
   D. All of the above

2. The _____ introduced the system software which provides the ability to load programs, move data to peripherals and libraries as well as to perform common computations.
   A. First generation computers
   B. Second generation computers
   C. Third generation computers
   D. Fourth generation computers

3. Which of the following is **FALSE** about secondary memory?
   A. Direct access from CPU is possible
   B. Has larger capacity
   C. The cost is cheaper
   D. Slower compared to primary memory

4. Which of the following is the most significant digit of 8532_{10}?
   A. 8
   B. 5
   C. 3
   D. 2

5. What is the value of 1.110_2 in decimal representation?
   A. 0.5_{10}
   B. 1.30_{10}
   C. 1.075_{10}
   D. 1.75_{10}

Continued.....

6. Which of the following shows -22_{10} in 8 bit sign-magnitude representation?
   A. $0001\ 0110_2$
   B. $1110\ 1001_2$
   C. $1001\ 0110_2$
   D. $1110\ 1010_2$

7. What is -6 in one's complement with 4-bit representation?
   A. 1001_2
   B. 1101_2
   C. 0110_2
   D. 1101_2

8. Which of the following types of instruction provides computational capabilities for processing numeric data?
   A. Arithmetic instruction
   B. I/O instruction
   C. Test instruction
   D. Branch instruction

9. Which of the following are the general categories of data?
   I. Addresses
   II. Numbers
   III. Characters
   IV. Logical data

   A. I, II and III
   B. I, II and IV
   C. II, III and IV
   D. All of the above

10. Which of the following are **TRUE** about EEPROM?
   I. It can be written into at any time without erasing prior contents
   II. Before a write operation, all the storage cells must be erased
   III. It combines the advantage of non-volatility with the flexibility of being updatable in place
   IV. It is more expensive than EPROM

   A. I, II and III
   B. I, II and IV
   C. I, III and IV
   D. II, III and IV

Continued.....

11. Figure 1 illustrates the _____ addressing mode.

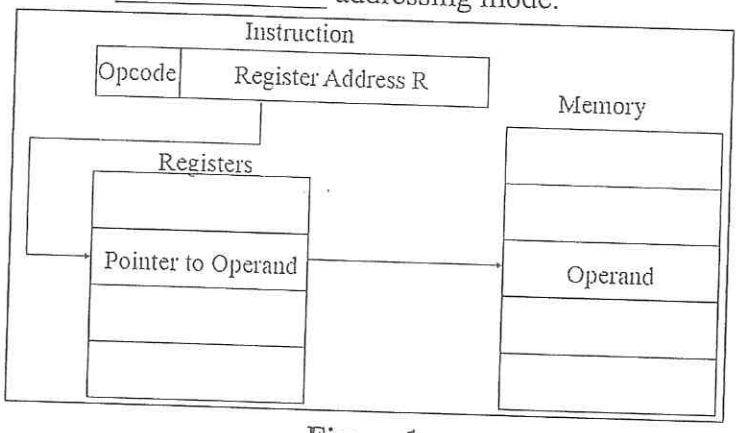

Figure 1

A. immediate
B. direct
C. register
D. register indirect

12. RAM technology is divided into two technologies: dynamic and static. Which of the following are **TRUE** about dynamic RAM?

I. It is made with cells that store data as charge on capacitors.
II. The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0.
III. It requires periodic charge refreshing to maintain data storage.
IV. The term dynamic refers to the tendency of the stored charge to leak away, even with power continuously applied.

A. I, II and III
B. I, II and IV
C. II, III and IV
D. All of the above

13. Which of the following are **TRUE** about sequential access method?

I. Memory is organized into units of data, called records.
II. Access must be made in a specific linear sequence.
III. Access time is variable.
IV. A word is retrieved based on a portion of its contents rather than its address.

A. I, II and III
B. I, II and IV
C. II, III and IV
D. All of the above

Continued.....

14. Second-level system bus that connects the memory subsystem to the chipset and processor is referred to as _____.
    A. cache bus
    B. memory bus
    C. local I/O bus
    D. standard I/O bus

15. Which of the following is **NOT** the common set of parallel wires of system bus?
    A. Address bus
    B. Control bus
    C. Data bus
    D. External bus

16. In programmed I/O, CPU has direct control over I/O. Which of the following tasks are directly controlled by CPU over I/O??
    I. Sensing status
    II. Read or write commands
    III. Wasting CPU time
    IV. Transferring data

    A. I, II and III
    B. I, II and IV
    C. I, III and IV
    D. II, III and IV

17. Which of the following I/O commands is used to activate a peripheral device and tell the device what to do?
    A. Control
    B. Test
    C. Write
    D. Read

18. In the following statement, *X* is referred to _____ technique.

> *X is a technique which provides a hardware poll. When the processor senses an interrupt, it sends out an interrupt acknowledge.*

    A. Multiple interrupt lines
    B. Bus arbitration
    C. Daisy chain
    D. Software poll

Continued.....

19. Which of the following is **NOT** type of pipeline hazard?
    A. data hazard
    B. control hazard
    C. resource hazard
    D. communication hazard

20. Which of the following are **TRUE** about pipelining?
    I. It is a key implementation technique used to build fast processors that can be seen in RISC architecture.
    II. It allows the execution of multiple instructions to overlap in time.
    III. It increases concurrency by dividing a computation into a number of steps.
    IV. In pipelined processing, the next instruction is processed after the entire processing of the previous instruction is complete.

    A. I, II and III
    B. I, II and IV
    C. II, III and IV
    D. All of the above

Continued.....

SECTION B: STRUCTURED QUESTIONS (60 Marks)

Instruction: *Answer ALL the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) List and briefly explain any **FOUR (4)** registers associated with processes done in the control unit or the ALU. [6 Marks]

b) Use an 8-bit binary representation to show how $26_{10} - 47_{10}$ is calculated. [7 Marks]

c) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert $E7A.0C_{16}$ to a normalised binary value. [2 Marks]
ii. Convert 725.302_8 to its hexadecimal equivalent. [3 Marks]
iii. Convert 417.21_8 to its decimal equivalent. [2 Marks]

QUESTION 2 (20 Marks)

a) Given the following expression,

$$X = [(G + E) * A] - [H * (A + S / L)]$$

i. Convert the expression to postfix notation. [1 Mark]
ii. Write the following machine instructions:
- One-address [2.5 Marks]
- Two-address [2 Marks]
- Three-address [1.5 Marks]

iii. Draw the stack diagrams that illustrate the program execution. [3 Marks]

Continued.....

b) A computer system has a memory architecture made up of main memory of 950MB and cache of 512KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 64 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping [3.5 Marks]
ii. Four-Way Set Associative Mapping [3.5 Marks]
iii. Associative Mapping [3 Marks]

QUESTION 3 (20 Marks)

a) Explain the operation of a bus in the computer system. [4 Marks]

b) When the processor, memory and I/O share a common bus, I/O devices can be interfaced with processor in two ways. State and explain the **TWO (2)** I/O interfacing techniques. [6 Marks]

c) Given **FOUR (4)** instructions where each instruction has **THREE (3)** stages (FI, DI, and EI) with delays of 5, 3, and 4 seconds for each stage respectively.

i. Draw a timing diagram for instruction pipeline operation. [4 Marks]

ii. Calculate the **total processing time**, **speedup** and **throughput** for the implementation of pipelining and non-pipelining. [6 Marks]
[Note: Please write the formula that is appropriate to use]

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